

MAC97(A)(B) SERIES

BIDIRECTIONAL THYRISTORS

FEATURES

- Available as "HR" (high reliability) screened per MIL-PRF-19500, JANTX level. Add "HR" suffix to base part number.
- Available as non-RoHS (Sn/Pb plating), standard, and as RoHS by adding "-PBF" suffix.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak repetitive off-state voltage⁽¹⁾ ($T_j = -40$ to $+110^\circ\text{C}$, $\frac{1}{2}$ sine wave 50 to 60Hz, gate open) MAC97-1, MAC97A-1, MAC97B-1 MAC97-2, MAC97A-2, MAC97B-2 MAC97-3, MAC97A-3, MAC97B-3 MAC97-4, MAC97A-4, MAC97B-4 MAC97-5, MAC97A-5, MAC97B-5 MAC97-6, MAC97A-6, MAC97B-6 MAC97-7, MAC97A-7, MAC97B-7 MAC97-8, MAC97A-8, MAC97B-8	V_{DRM}	30 60 100 200 300 400 500 600	Volts
RMS on-state current (full sine wave, 50 to 60Hz, $T_c = 50^\circ\text{C}$)	$I_{\text{T(RMS)}}$	0.6	Amps
Peak non-repetitive surge current (1 cycle, 60 Hz, $T_c = 110^\circ\text{C}$)	I_{TSM}	8.0	Amps
Circuit fusing considerations ($T_j = -40$ to $+110^\circ\text{C}$, $t = 8.3\text{ms}$)	I^2t	0.26	A^2s
Peak gate voltage ($t \leq 2.0\mu\text{s}$)	V_{GM}	5.0	Volts
Peak gate power ($t \leq 2.0\mu\text{s}$)	P_{GM}	5.0	Watts
Average gate power ($T_c = 80^\circ\text{C}$, $t = 8.3\text{ms}$)	$P_{\text{G(AV)}}$	0.1	Watts
Peak gate current ($t \leq 2.0\mu\text{s}$)	I_{GM}	1.0	Amps
Operating junction temperature range	T_j	-40 to +110	$^\circ\text{C}$
Storage temperature range	T_{stg}	-40 to +150	$^\circ\text{C}$

Note 1: V_{DRM} for all types can be applied on a continuous basis. Blocking voltage shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Maximum	Unit
Thermal resistance, junction to case	$R_{\theta\text{JC}}$	75	$^\circ\text{C}/\text{W}$
Thermal resistance, junction to ambient	$R_{\theta\text{JA}}$	200	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

Characteristic	Symbol	Min	Typ.	Max	Unit
Peak blocking current ⁽²⁾ (Rated V_{DRM} @ $T_j = 110^\circ\text{C}$)	I_{DRM}	-	-	0.1	mA
Peak on-state voltage (either direction) ($I_{TM} = 0.85\text{A}$ peak, pulse width ≤ 2 ms, duty cycle $\leq 2\%$)	V_{TM}	-	-	1.9	Volts
Gate trigger voltage (continuous dc) ($V_D = 12\text{V}$, $R_L = 100\Omega$) MT2(+),G(+) MT2(+),G(-) MT2(-),G(-) MT2(-),G(+) ($V_D = \text{Rated } V_{DRM}$, $R_L = 10\text{k}\Omega$, $T_j = 110^\circ\text{C}$) MT2(+),G(+); MT2(+),G(-); MT2(-),G(-) MT2(-),G(+)	V_{GT}	- - - - 0.1 0.1	- - - - - -	2.0 2.0 2.0 2.5 - -	Volts
Holding current (either direction) ($V_D = 12\text{V}$, gate open, $I_T = 200\text{mA}$)	I_H	-	-	10	mA
Gate controlled turn on time ($V_D = \text{rated } V_{DRM}$, $I_{TM} = 1.0\text{A}$ peak, $I_G = 25\text{mA}$)	t_{gt}	-	2.0	-	μs
Critical rate of rise of commutation voltage ($V_D = \text{Rated } V_{DRM}$, $I_{TM} = 0.84\mu\text{A}$ peak, commutating $di/dt = 0.32\text{A/ms}$, gate unenergized, $T_C = 50^\circ\text{C}$)	$dv/dt(c)$	-	5	-	$\text{V}/\mu\text{s}$
Critical rate of rise of off-state voltage ($V_D = \text{Rated } V_{DRM}$, exponential waveform, $T_C = 110^\circ\text{C}$)	dv/dt	-	25	-	$\text{V}/\mu\text{s}$

Note 2: Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

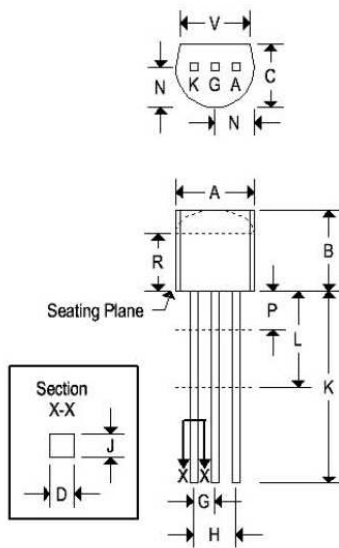
Quadrant and polarity	MAC SERIES			Unit
	97	97A	97B	
I MT2(+), G(+)	10	5.0	3.0	mA
II MT2(+), G(-)	10	5.0	3.0	mA
III MT2(-), G(-)	10	5.0	3.0	mA
IV MT2(-), G(+)	10	7.0	5.0	mA

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BIDIRECTIONAL THYRISTORS

MECHANICAL CHARACTERISTICS

Case	TO-92
Marking	Alpha-numeric
Pin out	See below



	TO-92			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.175	0.205	4.450	5.200
B	0.170	0.210	4.320	5.330
C	0.125	0.165	3.180	4.190
D	0.016	0.022	0.410	0.550
F	0.016	0.019	0.410	0.480
G	0.045	0.055	1.150	1.390
H	0.095	0.105	2.420	2.660
J	0.015	0.020	0.390	0.500
K	0.500	-	12.700	-
L	0.250	-	6.350	-
N	0.080	0.105	2.040	2.660
P	-	0.100	-	2.540
R	0.115	-	2.930	-
V	0.135	-	3.430	-

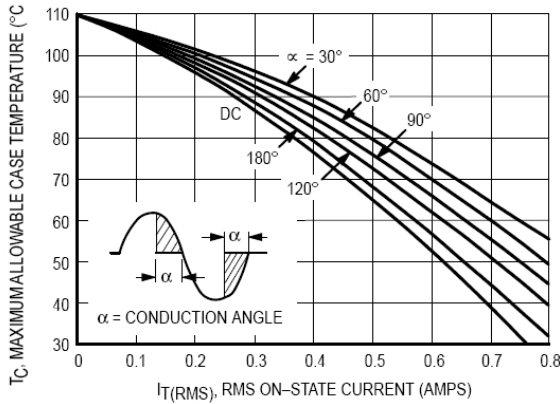


Figure 1. RMS Current Derating

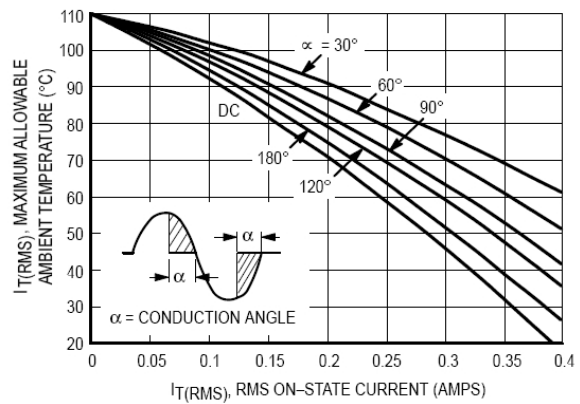


Figure 2. RMS Current Derating

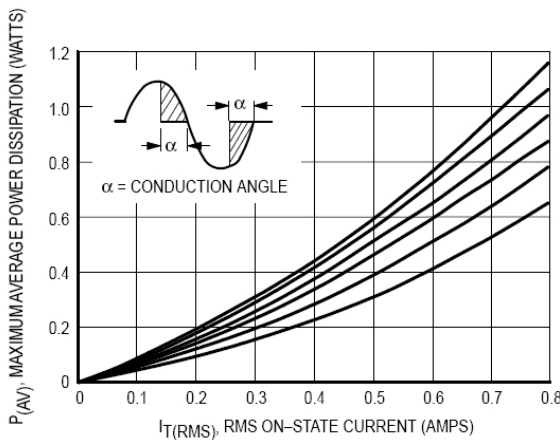


Figure 3. Power Dissipation

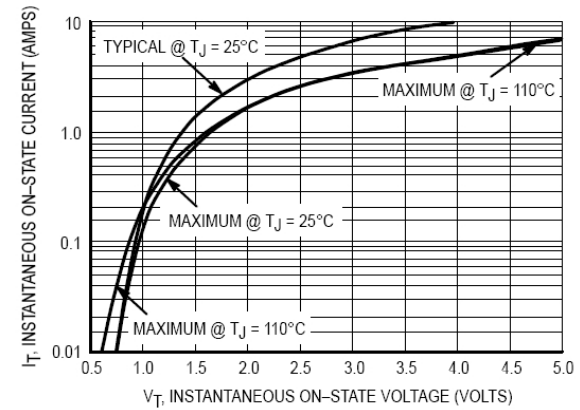


Figure 4. On-State Characteristics

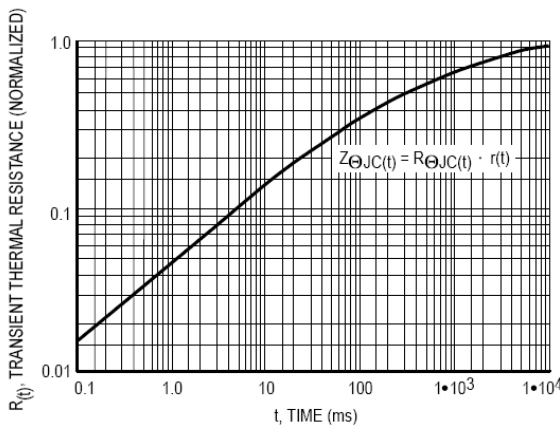


Figure 5. Transient Thermal Response

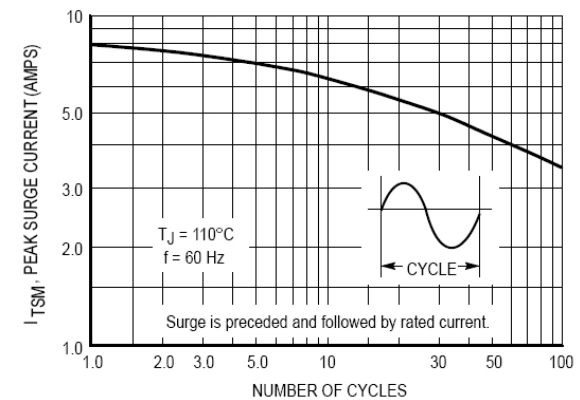


Figure 6. Maximum Allowable Surge Current

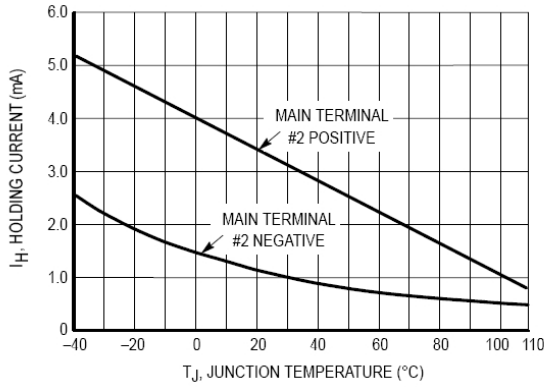


Figure 7. Typical Holding Current Variation

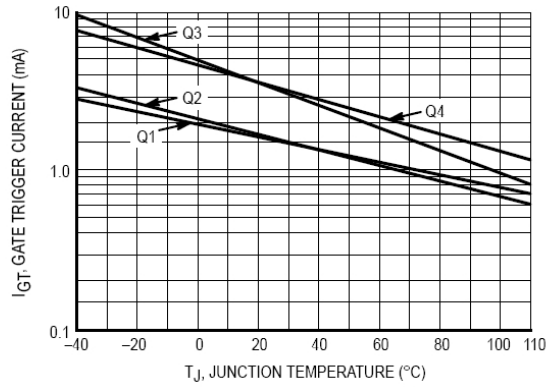


Figure 8. Typical Gate Trigger Current Variation

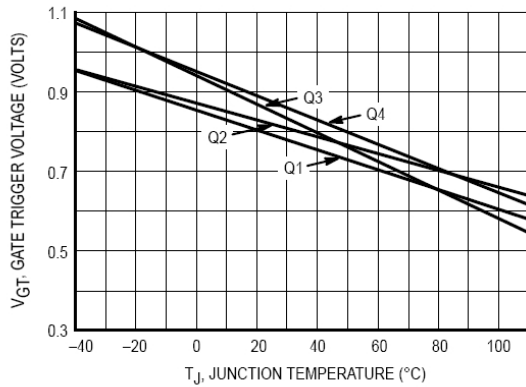


Figure 9. Gate Trigger Voltage Variation

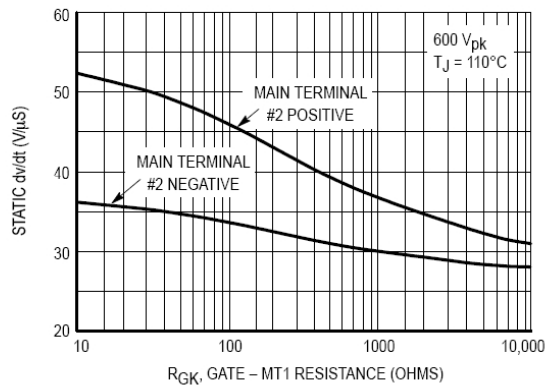


Figure 10. Exponential Static dv/dt versus Gate - MT1 Resistance

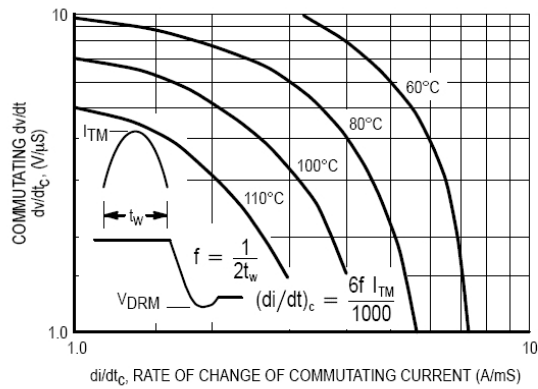


Figure 11. Typical Commutating dv/dt versus Current Crossing Rate and Junction Temperature

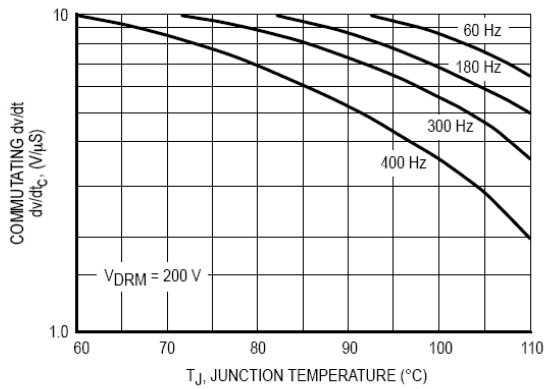
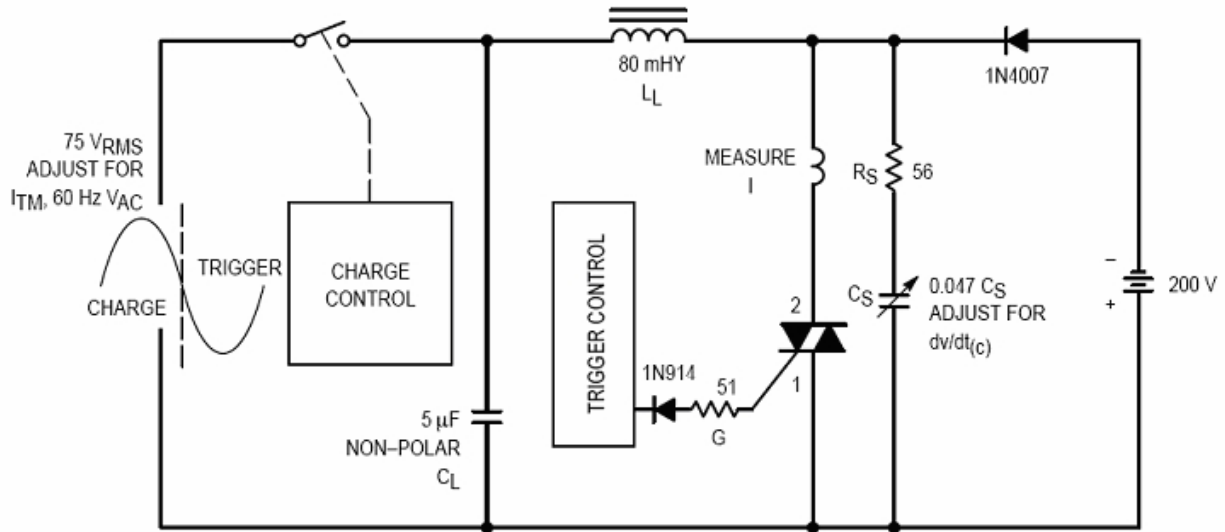


Figure 12. Typical Commutating dv/dt versus Junction Temperature at 0.8 Amps RMS



NOTE: Component values are for verification of rated $(dv/dt)_C$.

Figure 13. Simplified Q_1 $(dv/dt)_C$ Test Circuit